REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-17 are currently under consideration. Claims 18-26 have been withdrawn from consideration. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

Telephone Interview

Applicants note with appreciation the courtesies extended by Examiner Fenty on November 26, 2003 in a telephone interview. During that discussion, Applicants again tried to explain why Figure 10 of the Jun et al. reference was inconsistent with the remainder of the reference and therefore should be disregarded. No agreement was reached during the interview.

Art Rejections

The claims the Examiner rejected as being either anticipated by or obvious over Jun et al. (U.S. Patent No. 6,406,948), either alone or in combination with Watt (U.S. Patent No. 5,623,156). These rejections are respectfully traversed.

Applicants again point out that Figure 10 of the Jun et al. reference, which is at the center of the rejections, does not show the present invention. In particular, the Examiner cites this

Figure to show the stacked diode. However, Applicants submit that there is no description of this arrangement other than in the Figure itself and that the Figure is contrary to the teachings of the rest of the specification and accordingly must be considered a mistake.

A description in Figure 10 is found in column 2, lines 31 and 32 in the Brief Description of the Drawings which merely indicates that it is a schematic representation of the electrostatic discharge protection network of the invention. The only other description is found at column 3, lines 57-59 which further states that the numbered areas relate to Figure 9. Thus, there is no description of these diodes in the written specification. The Figure shows four pairs of diodes connected in series. If this depiction were in agreement with the rest of the specification, and especially Figure 9, it could be used as a valid reference. However, Figure 10 is contrary to the teachings of the remainder of the specification and accordingly should be considered an erroneous drawing.

Applicants submitted a marked-up copy of Figure 9 of the reference in the Amendment filed May 12, 2003. The markings on that Figure indicated the location of diodes which are formed by the various regions of the ESD device of the reference. If these

diodes are then formed into a schematic in the same fashion as Figure 10, they would form the equivalent circuit shown in the attached Figure. In this circuit, the diodes are all connected in a similar fashion to Figure 10, but are formed all in parallel rather than in series. Thus, the remainder of the specification would indicate that the diodes are connected in parallel rather than in series. Since there is no description of the series connection except for the Figure, it is assumed that the Figure is in error and that the depiction should be that of a parallel configuration.

As shown in the two Figures, all of the diodes in Figure 9 are connected in parallel between the I/O pad and the power rail. These indicate that the nodes have a single diode connected in parallel. Since Figure 9 and the rest of the specification indicates that these diodes should be shown in parallel, it would not appear that the series connections of Figure 10 are correct. Further, it is not considered reasonable that the diodes in Figure 10 would be added in addition to the diodes of Figure 9. Not only is there no comment about this in the specification, but in addition, they would be redundant. In particular, a single diode would be turned on earlier than the stacked diodes when forward biased and a single diode will be broken down earlier than the

stacked diodes when reverse biased. Thus, adding such stacked diodes to the single diode would not only be meaningless, but waste space on a chip. Accordingly, one skilled in the art would realize when viewing this Figure that the diodes are incorrectly depicted and that therefore the reference does not disclose the use of stacked diodes in this arrangement.

As shown in Figure 6, and described in the corresponding specification, Applicants utilize the stacked structure in order to lower the value of the parasitic capacitance. Jun et al. and the other references do not teach the need to lower the parasitic capacitance to obtain better results and this would not be obvious without the reference to the present specification. Accordingly, Applicants submit that the present claimed invention is neither anticipated by nor obvious over the Jun et al. reference.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejection, and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully

requested to contact the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicants respectfully petition for a one (1) month extension of time for filing a response in connection with the present application and the required fee of $110.00 is included in the check for the Notice of Appeal which is being filed concurrently herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Joe McKinney Muncy, #32,334

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

KM/RFG/ags
0941-0316P

Attachment(s): Marked-up Figures 9 and 10